Fig. 1

Fig. 2
(Prior Art)

Bit Time	7	6	5	4	3	2	1	0
1			CMD[5:0]					
2								
3								
4								

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Fig. 3

Bit Time	7	6	5	4	3	2	1	0
1	SrcUnit [1:0]		CMD[5:0]					
2	DestNode[2:0]			DestUnit [1:0]		SrcNode[2:0]		
3				SrcTag[4:0]				
4								
5	Addr[15:8]							
6	Addr[23:16]							
7	Addr[31:24]							
8	Addr[39:32]							

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Fig. 4
(Prior Art)

Bit Time	7	6	5	4	3	2	1	0
1	SrcUnit [1:0]		CMD[5:0]					
2	DestNode[2:0]			DestUnit [1:0]		SrcNode[2:0]		
3				SrcTag[4:0]				
4								

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Fig. 5

Bit Time	7	6	5	4	3	2	1	0
1	Data[7:0]							
2	Data[15:8]							
3	Data[23:16]							
4	Data[31:24]							
5	Data[39:32]							
6	Data[47:40]							
7	Data[55:48]							
8	Data[63:56]							

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Fig. 6
(Prior Art)

CMD Code	Command	Packet Type
000000	Nop	Info
000001	VicBlk	Command/Data
000010	Reserved	
000011	ValidateBlk	Command
000100	RdBlk	Command
000101	RdBlkS	Command
000110	RdBlkMod	Command
000111	ChangetoDirty	Command
x01xxx	WrSized	Command/Data
01xxxx	ReadSized	Command
100xxx	Reserved	
110000	RdResponse	Response/Data
110001	ProbeResp	Response
110010	TgtStart	Response
110011	TgtDone	Response
110100	SrcDone	Response
110101	MemCancel	Response
11011x	Reserved	
11100x	Probe	Command
11101x	Broadcast	Command
11110x	Reserved	
111110	Reserved	
111111	Sync	Info

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Fig. 7

Fig. 8

to Packet
Processing
Logic 58

from Packet
Processing
Logic 58

to/from Packet
Processing Logic
58

SrcDone

Command Packets

Probe

Request Queue 60							
V	Type	SrcNode	SrcUnit	SrcTag	Addr	Data	State

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Memory Access
Control Circuit
66

Partial Directory
Cache
62

Coherency
Control
Circuit
64

Data

MC 16A

to Memory 14A
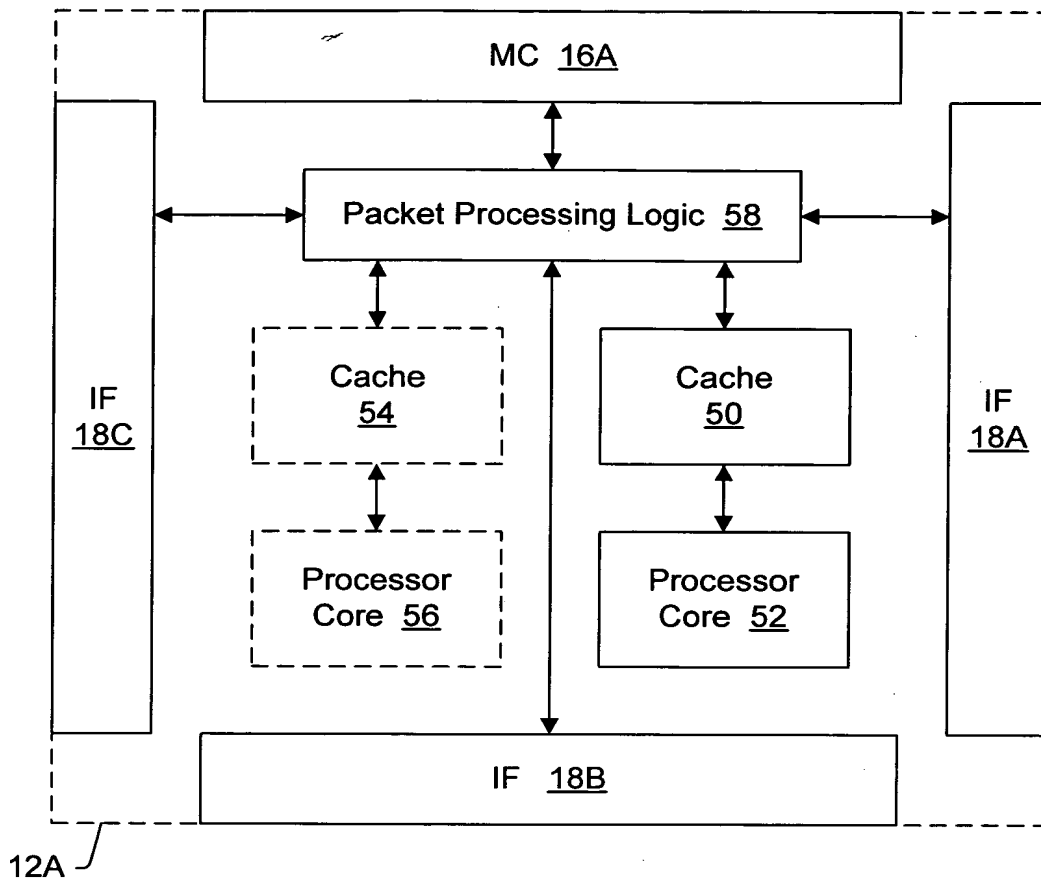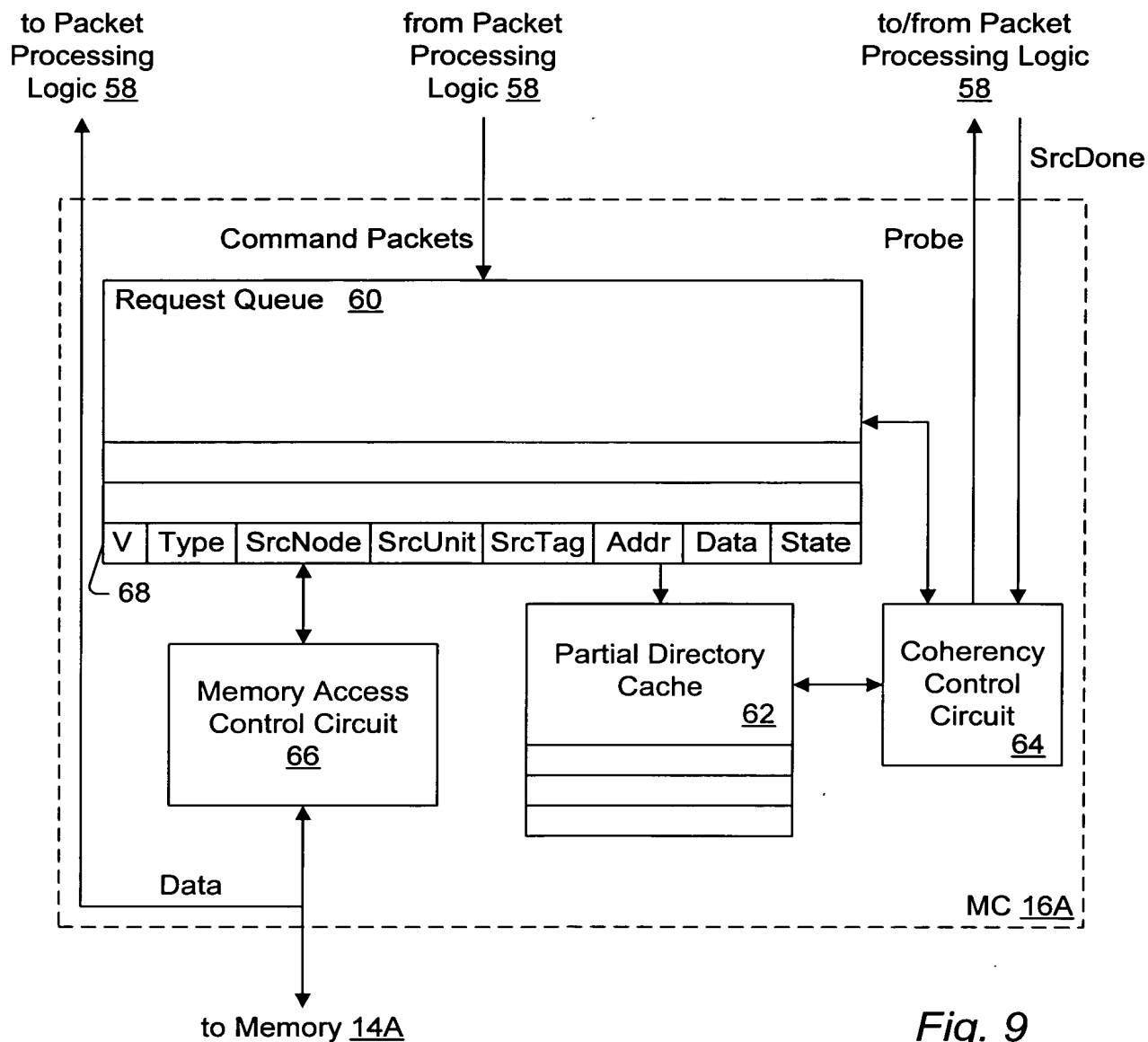
Fig. 9
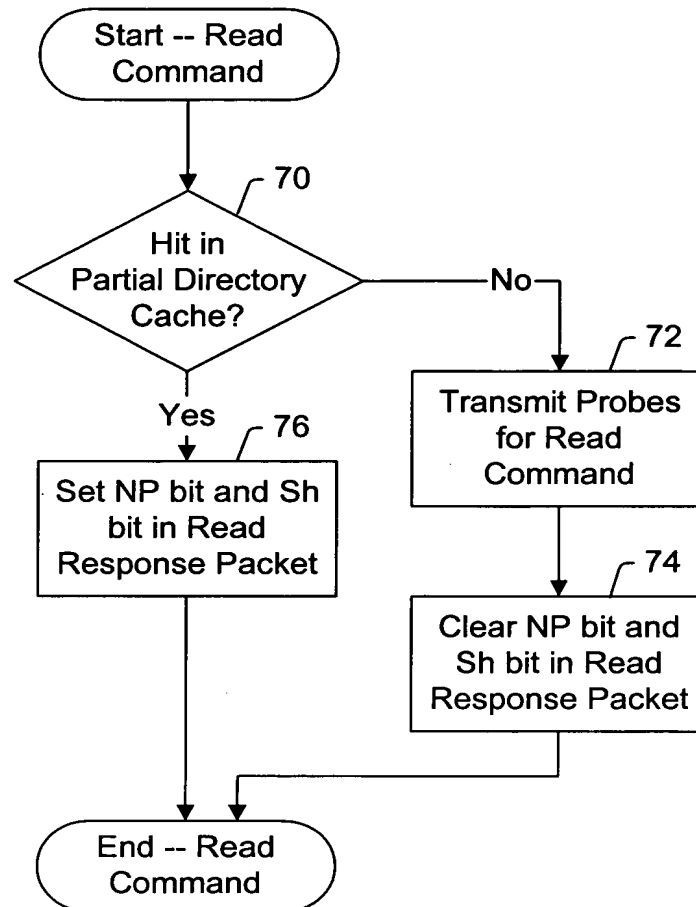
Fig. 10
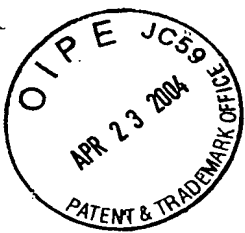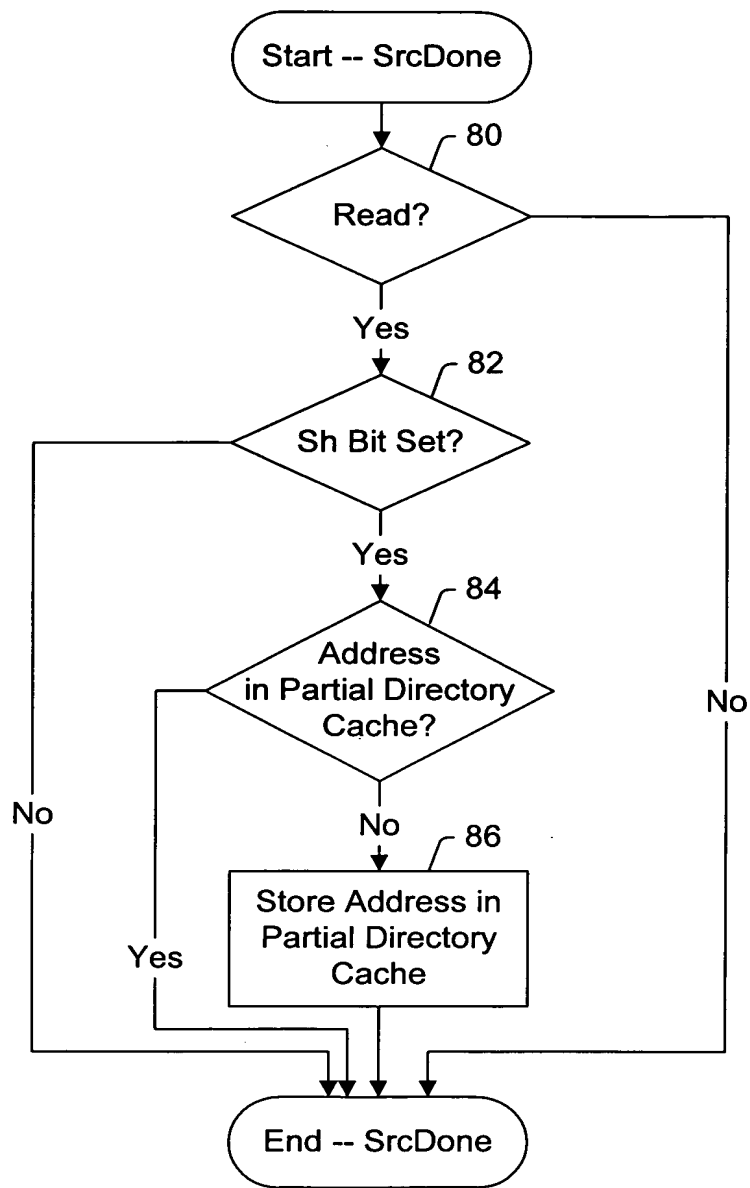
Fig. 11
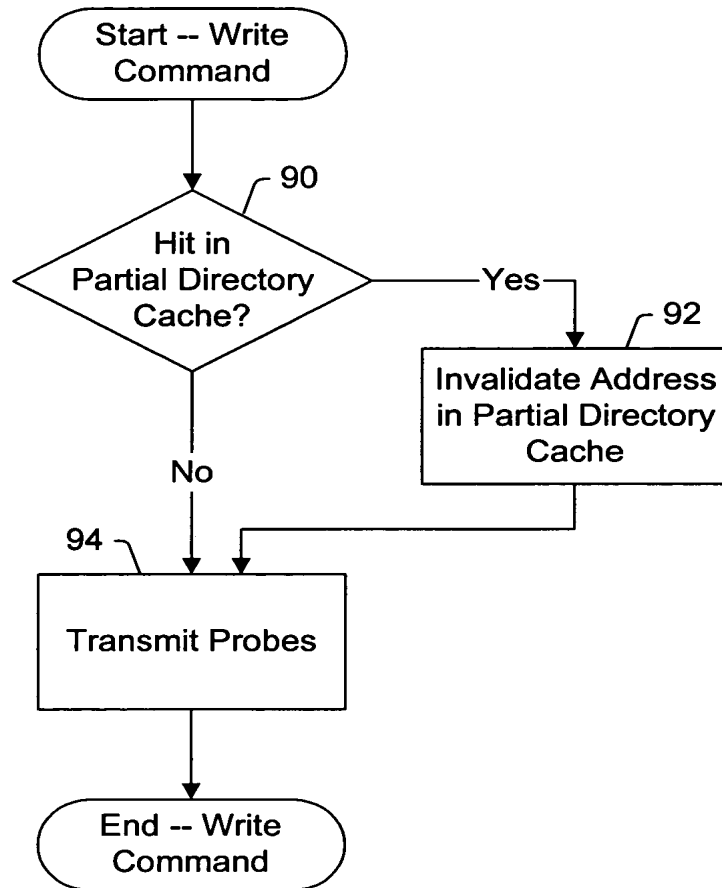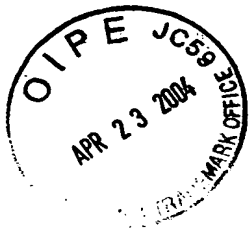
Fig. 12
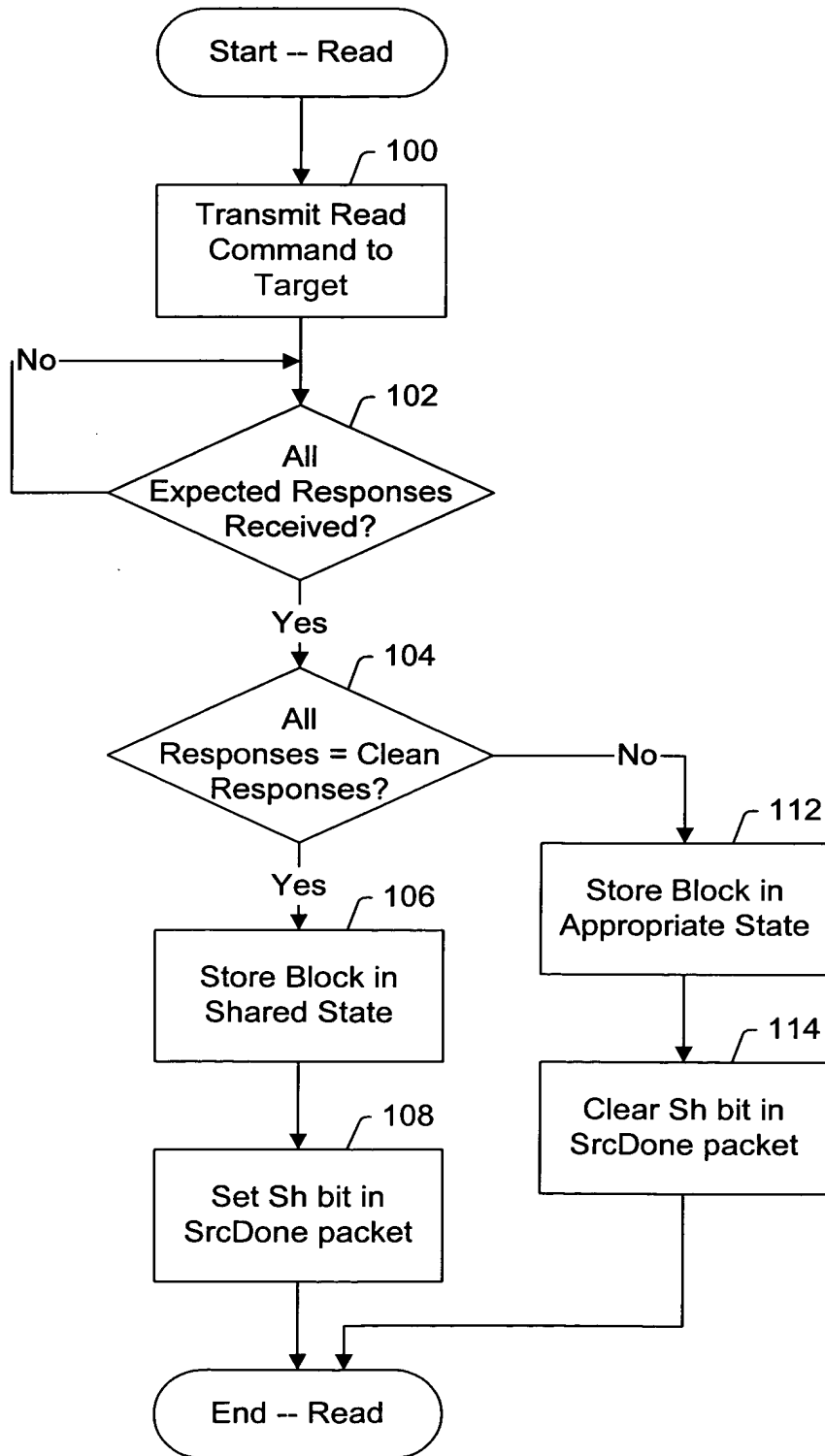
Fig. 13

V	Page Address	B0V	B1V	B2V	B3V	. . .	B63 V

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Fig. 14

Bit Time	7	6	5	4	3	2	1	0
1	SrcUnit [1:0]		CMD[5:0]					
2	DestNode[2:0]			DestUnit [1:0]		SrcNode[2:0]		
3				SrcTag[4:0]				
4	Sh							

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Fig. 15

Bit Time	7	6	5	4	3	2	1	0
1	SrcUnit [1:0]		CMD[5:0]					
2	DestNode[2:0]			DestUnit [1:0]		SrcNode[2:0]		
3	Count[1:0]		Err	SrcTag[4:0]				
4	Sh	P	NP			Cncl	Count[3:2]	

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Fig. 16